What is claimed is:

1. An In-System-Developer (ISD) for developing a customized integrated circuit (IC) for use in an external system while connected to the external system, the ISD comprising:

a development board for holding an IC core, the development board having a one or more ports for transmitting data and signals to and from the IC core;

a data processing system coupled to the development board;

hardware descriptor language (HDL) software capable of being executed by the data processing system to configure the IC core to form the IC;

at least one input-output (IO) cable coupling the ports to the external system for transmitting data from the external system to the IC core and transmitting signals from the IC core to the external system; and

interface software having program code adapted to translate Register Transfer Level (RTL) code to code used by the HDL software, thereby enabling the design to be tested as it is being developed.

2. An ISD according to claim 1, wherein the interface software further comprises program code adapted to assign predetermined signal in the RTL code to predetermined ports on the development board.

3. An ISD according to claim 1, wherein is using a Universal Test & Operations Physical Interface for ATM (UTOPIA) interface and wherein the interface software is adapted to translate UTOPIA RTL code.

4. An ISD according to claim 1, wherein the interface software comprises program code adapted to enable assigning a clock speed for the IC core.

5. An ISD according to claim 4, wherein the interface software comprises program code adapted to determine if the IC core is capable of operating at the assigned clock speed.

6. An ISD according to claim 1, wherein the interface software comprises

program code adapted to enable designating ports on the development board to be monitored.

7. An ISD according to claim 6, wherein the interface software comprises program code adapted to enable designating an output to be recorded in a VCD file.

8. An ISD according to claim 1, wherein the IC core is selected from a group consisting of:

Field Programmable Gate Arrays; and

Electronically Reconfigurable Gate Arrays.

9. A method for developing a integrated circuit (IC) for use in an external system while connected to the system, the method comprising steps of:

mounting an IC core in a development board having a one or more ports for transmitting signals to and from the IC core;

coupling the development board to a data processing system;

coupling the one or more ports to the external system;

executing on the data processing system hardware descriptor language (HDL) software to configure the IC core to form the IC;

transmitting data between the external system and the IC core; and

translating Register Transfer Level (RTL) code to code used by the HDL software using interface software, whereby a design of the IC is tested as it is being developed.

10. A method according to claim 9, further comprising the step of assigning predetermined signals in the RTL code to predetermined ports on the development board using the interface software.

11. A method according to claim 9, using a Universal Test & Operations Physical Interface for ATM (UTOPIA) interface and wherein the step of translating RTL code comprising the step of translating UTOPIA RTL code.

12. A method according to claim 9, further comprising the step of assigning a

clock speed at which the IC core is tested using the interface software.

13. A method according to claim 12, further comprising the step of prior to assigning a clock speed determining if the IC core is capable of operating at the assigned clock speed.

14. A method according to claim 9, further comprising the step of designating from which ports signal are to be recorded in a VCD file.

15. A method according to claim 9, further comprising the step of generating a test bench using data in the VCD file to enable self-checking of the IC core.

16. A computer program product for developing a integrated circuit (IC) for use in an external system while connected to the system, the computer program product comprising a computer readable storage medium and a computer program mechanism embedded therein, the computer program mechanism, comprising:

a program module that directs a data processing system coupled to a development board having an IC core held therein, to function in a specified manner, to translate Register Transfer Level (RTL) code to code used by hardware descriptor language (HDL) software to configure the IC core to form the IC, thereby enabling the design to be tested as it is being developed.

17. A computer program product according to claim 16, wherein the program module includes program code for assigning predetermined signals in the RTL code to predetermined ports on the development board.

18. A computer program product according to claim 16, using a Universal Test & Operations Physical Interface for ATM (UTOPIA) interface and wherein the program module includes program code for translating UTOPIA RTL code.

19. A computer program product according to claim 16, wherein the program module includes program code for assigning a clock speed for the IC core.

20. A computer program product according to claim 19, wherein the program module includes program code for determining if the IC core is capable of operating at the assigning clock speed.

21. A computer program product according to claim 15, wherein the program module includes program code for designating the ports on the development board to be monitored.

22. A computer program product according to claim 21, wherein the program module includes program code for designating an output to be recorded in a VCD file.